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PATENT APPLICATION

531 Rec'd PCT/PTO 26 APR 2001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#3 10/22/01

In re the Application of

Makoto KOBAYASHI and Hiroyuki TAKAMATSU

Application No.: US National Stage of PCT/JP00/05595

Filed: April 26, 2001 Docket No.: 109352

For: POLISHING PAD AND POLISHING METHOD FOR SEMICONDUCTOR WAFER

PRELIMINARY AMENDMENT

Director of the U.S. Patent and Trademark Office
Washington, D. C. 20231

Sir:

Prior to initial examination, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 1-10 without prejudice to or disclaimer of the subject matter contained therein.

Please add new claims 11-31 as follows:

--11. A polishing pad used for polishing a semiconductor wafer in a mirror polishing process, wherein a content of zinc compounds included in the polishing pad is 200ppm or less at the ratio of zinc weight relative to the weight of the polishing pad.--

--12. A polishing pad used for polishing a semiconductor wafer in a finish polishing process, wherein a content of zinc compounds included in the polishing pad is 100ppm or less at the ratio of zinc weight relative to the weight of the polishing pad.--

--13. A polishing pad used for polishing a semiconductor wafer in a finish polishing, wherein the polishing pad does not include zinc compounds.--

--14. The polishing pad used for polishing a semiconductor wafer according to Claim 11, which comprises a base layer formed of nonwoven fabric and a porous surface layer.--

--15. The polishing pad used for polishing a semiconductor wafer according to Claims